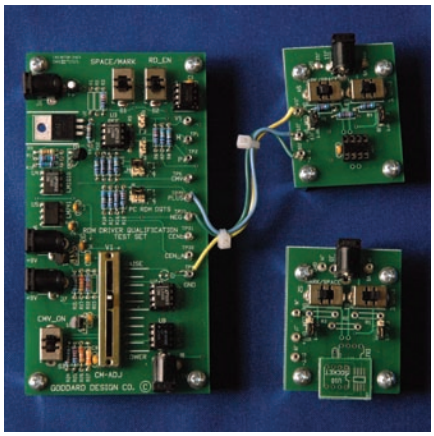

RDM's physical layer: Testing transceivers and bias networks

BY **ROBERT GODDARD**

SUCCESSFULLY IMPLEMENTING RDM is more than a code project. Getting an E1.20 device to work on a lab bench or at a Plugfest may be reasonably straightforward, but in the real world of long cable runs, multiple devices, and electronic interference, the correct implementation of RDM's physical layer is important. Transceivers and bias networks that can pass the tests written into *ANSI E1.20, Remote Device Management Over DMX512 Networks*, are critical for proper RDM network functioning.

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RDM's physical layer requirements are described in ANSI E1.20 and in ANSI E1.11, the DMX512-A standard. E1.20 puts requirements on the line interface that go beyond those of ANSI E1.11 or the earlier DMX512/1990. The most obvious is that transceivers must be configured for bidirectional operation, but the less obvious requirements are:

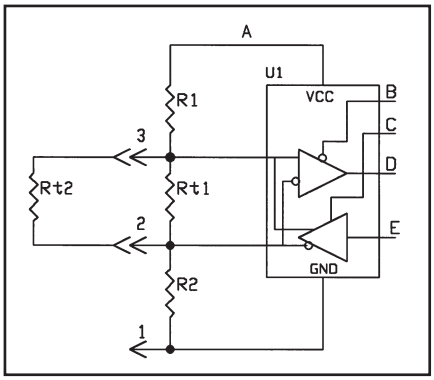
- Transceivers for command ports (controllers and outputs of splitters) need a Line Bias Network to keep the line in a marking state when idle.
- All transceivers on an RDM data line segment must be tri-stated between each RDM request and reply message. If there were not a guaranteed period when all line drivers were switched to tri-state, there would be data collisions that could mimic Null START Code traffic, producing the dreaded flicker.
- RDM data line segments must be terminated at both ends. RDM devices transmitting in the middle of a data line will issue an electrical signal, which propagates toward both ends of the segment. Unless each end of the cable segment is properly terminated, the signal can echo off each end.
- Transceivers for command port and responder port designs must be verified by tests described in the E1.20 standard. This verification requires the use of a specialized test set described in the standard.

What are the requirements for this Line Bias Network? Quoting from the E1.20 standard:

> ***2.4.1 Line Bias Networks***
>
> *The command port shall provide a means to bias the termination of the data link to a value of at least 245 mV and verified by using the test circuit described in Appendix F. This means may be disabled for special applications. If the line biasing network is enabled, the differential input impedance shall be 120 ohms +/- 10%; however, if it is not enabled, the differential input impedance shall not be greater than one unit load.*
>
> *The termination shall be polarized such that Data+ of the data link is positive with respect to Data- of the data link. The Line Biasing Network shall maintain this bias when the data link is loaded with the equivalent of 32 unit loads and common mode voltage is varied over the range of +7 volts to -7 volts DC.*

The Line Bias Network greatly decreases the error rate on the RDM line. The EIA-485 standard says all receivers must output a 1 for an input of at least 200mV. While most chips are more sensitive than required by 485, the RDM required value is a safe value to design to. The E1.20 standard gives a reference circuit. The use of this circuit is not required. Any design that produces the same results is allowed. However, many designs use some variation of the reference design because it is simple and it works.

During development of the RDM standard several objections were made to



LINE BIAS NETWORK REFERENCE CIRCUIT RESISTOR VALUES		
R1	562 Ω 2%	
R2	562 Ω 2%	
Rt1	133 Ω 2%	Rt1 parallel (R1+R2) should equal 120 Ω
Rt2	120 Ω 5%	This resistor is not physically part of the Line Bias Network. It should be located at the opposite end of the data link from the command port.
Vcc	+5 VDC	Resistor values above assume 5VDC operation. Other Vcc values will require new resistor value calculations.

the Line Bias Network as a solution for keeping the line in a marking state when idle. One was "I can use some of the new 485-style drivers that have been designed to solve the problem of floating inputs. I buy the right chip and I am done!"

If RDM had been a clean sheet of paper design and we had been willing to tie the standard to a particular single source chip, mandating particular drivers might have been a choice. However, the RDM standard can't use this solution because it works only if all the chips in the lighting system are of this type. This would destroy compatibility with all the legacy DMX512 products in the field!

Another objection was that use of this network violates the loading rules of EIA-485. At first look, it does. If an EIA-485 driver can only just drive the required 31 additional unit loads, and you then strap on the pull-up and pull-down resistors, the output is not going to meet the 485 rules.

The black box model to the rescue

However, most real-world drivers will drive that many unit loads and the bias network. But not all. This is why there are design verification tests in the E1.20 standard. An integrated circuit is a classic black box. Very few of us know what is inside the black blob of epoxy. The details are not published. Two different chip numbers may be totally interchangeable but have very different circuit topologies. All we can do is probe the black box from the outside. If we add some extra parts to our black box circuit model, and if the combined circuit still passes certain critical tests, then it can still be used to drive the number of unit loads required by EIA-485. The driver and the external parts are now a biased 485 driver. Luckily for RDM, most 485 drivers are considerably over designed.

The tests and what they mean

The tests laid out in the RDM standard are for design verification; they are **not** required as production tests. The standard is reasonably clear on how to do the tests. It is not that good at explaining how to use the data. What follows are summaries of the tests in Appendix F of E1.20, and some guidance on interpreting the data.

Test 1, passive bias measurement

Test 1 in clause F.2 measures the ability of the proposed bias network to provide the appropriate bias to the inactive cable segment. The segment is terminated, loaded by 31 additional unit loads, and subjected to common mode voltage varying between +7 and -7 volts. Note that the center point of the common mode voltage is offset by 1.8 volts, which is more or less the signal offset of most 5 volt drivers. This test measures the behavior of the network and the power supply and any protection components. The choice of a transceiver has little effect on the results of this test. We used the same bias network in testing 16 different transceivers. To pass this test the bias must be 245 mV or greater. While no top limit is set, another test will limit this value.

Test 2, active drive level

Test 2 in clause F.2 measures the ability of the transceiver chip to drive a mark or space onto the line when loaded with the same test load used for test 1. This test should be done with the exact circuit that will be used in production. However, how a transceiver chip behaves with a compliant bias network can be used to predict how it will work with a similar compliant network. To pass, the driver must provide a differential drive of at least + or - 1.5 volts. Many of the chips we have tested passed this test by a wide margin. Median output was 2.365V.

Test 3, driver symmetry

Ideally, the mark and space outputs of a driver are of identical amplitude. However, adding a pull up resistor to the positive output while adding a pull down resistor to the negative output cannot help but decrease the symmetry of the waveform. The positive (mark) output will be larger and the negative (space) will be smaller. Test 3 in clause F.2 measures the asymmetry of the output waveform. Passing requires that asymmetry be less than 200 mV. Asymmetry decreases the apparent signal strength of one state by twice the asymmetry. This is the only test that we have found that poses a problem for standard EIA-485 chips. We have seen three chips fail this test.

Test 4, base line shift

Test 3 in F.2 has a second part. The outputs of EIA-485 drivers float above the zero-volt rail. Your classic 5-volt driver design has a minimum output voltage of about 1.5 to

2 volts above the common rail. This base line is much lower for 3.3 volt designs. The second part of test 3 in F.2 measures the shift of this base line voltage. To pass, the shift must be less than 200 mV. We have yet to see a chip that fails this test.

are equal to or exceed the values measured for the calibration network, the proposed network does not overload the line.

A network that passes the tests in clauses F.1 through F.3 meets the requirements of the standard. It should also be noted that if the value for the calibration network is recorded for a particular test set, the calibration needs to be done only once.

SN75176				
CONTROLLER TESTS				Limit
Common Mode Voltage	-7	0	+7	
Passive Bias	0.254 V	0.253 V	0.252 V	≥245 mV
Active Drive +	2.753 V	2.850 V	2.924 V	≥1.5 V
Active Drive -	-2.634 V	-2.736 V	-2.838 V	≥1.5 V
Symmetry		0.129 V		≤200 mV
Base line shift		0.016 V		≤200 mV
RESPONDER TESTS				
Common Mode Voltage	-7	0	+7	
Active Drive +	2.697 V	2.846 V	2.946 V	≥1.5 V
Active Drive -	-2.561 V	-2.718 V	-2.861 V	≥1.5 V
Asymmetry		0.126 V		≤200 mV
Base line shift		0.026 V		≤200 mV

If you wish to be sure that your RDM device will perform in a low error manner, qualifying the drivers is an essential step.

Test 5: Does the bias network overload responders?

So far the tests have not limited how much bias a controller port may place on the segment and all the attached responder ports. So, even if the responder can drive the reference design bias network, it might not be able to drive your design. The solution is to test your proposed network against a network that provides a slightly greater load than the reference design. Any good EIA-485 transceiver is now tested for its ability to drive a mark or space on both your proposed controller bias network and the calibration network specified in F.3. If your proposed network produces values whose magnitudes

Responder tests

Figure F-4 in clause F.4 of the standard shows the Responder Test Circuit set for qualifying responder transceivers. It consists of a doubly terminated 31-load simulator plus a maximal bias network. The tests using the Responder Test Circuit required in F.5 are essentially the same as tests 2, 3, and 4 outlined above.

What do real transceivers look like when tested to this standard?

In May 2010 Goddard Design ran the tests required by E1.20 on 16 different driver chips. The testing was done by Jessica Kleinbart, a high school intern at Goddard Design. The test set was our FD RDM DQTS driver qualification test set. I supervised the tests.

The results of these tests show that implementing the drivers required by E1.20 is possible without great gnashing of teeth. Only three chips failed any of the tests, and these three failed only one test by a small amount. At least some of the available 3.3 volt drivers meet the requirements of E1.20, too. The SN75176 table shows the test results for the SN75176 chip. The reason for showing the results for an SN75176 is that it was the default transceiver chip for DMX512 designs for many years. While now considered an antique design, it is clearly usable by RDM.

Today many other chip designs have been introduced with new and desirable features. Some draw less power, some present fractional unit loading, some have higher ESD protection, some will withstand up to a 60-volt bus fault continuously, and some are less particular about termination due to controlled slew rate outputs. Finally there are the chips that have offset thresholds to get around tri-stated line problems that RDM has solved by the bias network scheme. As is noted above, these chips do not help in most RDM systems.

The Summary Table gives the results for all the chips we tested. The results are interesting because all chips passed the active drive test. That is the test that, on first

SUMMARY TABLE				
	Largest	Median	Smallest	Limit
Active drive level, either polarity, any CMV	3.94 V	2.365 V	1.66 V	> 1.5 V
Asymmetry	265 mV	137 mV	77 mV	< 200 mV
Base line shift	56 mV	24.8 mV	4 mV	<200 mV

glance, would appear to be the hardest to pass. The most problematic parameter is asymmetry. It was noted that chips using the CMOS process were the ones demonstrating the most difficulty with asymmetry.

If you wish to be sure that your RDM device will perform in a low error manner, qualifying the drivers is an essential step. It requires the right test set, which can be built or bought, and about half an hour of your time. It should be considered a standard part of the design process, equal in importance to code verification. ■

Bob Goddard and Goddard Design Co. have designed and built theatrical lighting and automation control devices for over 40 years. Twenty years ago he introduced the Lil'DMXter, which set the standard for DMX512 testing. The current production DMXter4 RDM and the MiniDMXter4 are the most recent items in this family. Goddard Design offers hardware and software testing and consultation services for other manufacturers. Bob serves as a principal member of the Control Protocols Working Group.